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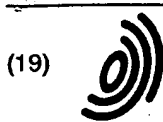
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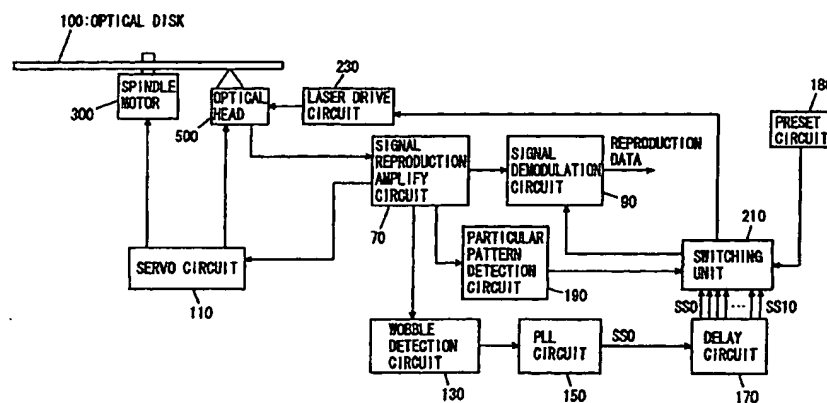
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(54) INFORMATION REPRODUCER, INFORMATION RECORDER AND REFERENCE MARK DETECTION CIRCUIT

(57) Information reproduction apparatus of the present invention is directed to realize data reproduction properly and reliably from an optical disk, including a wobble detection circuit (130) to detect a wobble signal read out by an optical head (500), a PLL circuit (150) to frequency-multiply the wobble signal to generate a synchronizing signal (SS0), a delay circuit (170) delaying a synchronizing signal (SS0) sequentially to generate a plurality of synchronizing signals (SS0-SS10) of differ-

ent phases, a particular pattern detection circuit (190) to detect a particular pattern in a reproduced signal, and a switching unit (210) to select one synchronizing signal having a phase difference preset by a preset circuit (180) with respect to a detected particular pattern and supplying the selected synchronizing signal to a laser drive circuit (230) and to a signal demodulation circuit (90).

FIG. 1



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Description

Technical Field

[0001] The present invention relates to an information recording reproduction apparatus that records information on a magneto-optical recording medium and that reproduces the recorded information from a magneto-optical recording medium.

Background Art

[0002] The development of a magneto-optical recording medium (referred to as "optical disk" hereinafter) is now intensive together with the recording and reproducing technique since it is a rewritable and reliable recording medium of a large storage capacity.

[0003] In a conventional magneto-optical recording reproduction apparatus, a synchronizing signal is pre-recorded magnetically at the beginning of every unit of data on an optical disk together with the data. By detecting that synchronizing signal at the time of reproduction for synchronization, the subsequent recorded data can be read out sequentially.

[0004] However, when the above-described pre-recorded synchronizing signal is missing in the reproduced signal according to the conventional recording/reproduction technique, there was a problem that the appropriate timing to direct a laser beam onto the optical disk for reproduction could not be established, so that data could not be reproduced reliably.

Disclosure of the Invention

[0005] An object of the present invention is to provide an information recording/reproduction apparatus that can realize data reproduction more correctly and reliably.

[0006] Another object of the present invention is to provide a reference mark detection circuit that can detect accurately with a simple structure a reference mark such as an address mark (referred to as "fine clock mark" hereinafter) formed together with the wobble at a groove.

[0007] According to an aspect, the object of the present invention is achieved by providing an information reproduction apparatus including an information readout circuit responsive to a supplied control signal to read out information from a mounted recording medium, a reproduction circuit demodulating information to generate reproduction data, a first period signal detection circuit detecting a first period signal from the read out information, a synchronizing signal generation circuit generating a plurality of synchronizing signals of different phases according to the detected first period signal, a second period signal detection circuit detecting a second period signal from the read out information, and a control circuit selectively supplying as a control signal to

the information read out circuit a synchronizing signal out of the plurality of synchronizing signals generated by the synchronizing signal generation circuit that has a predetermined phase difference with respect to the second period signal detected by the second period signal detection circuit.

[0008] According to another aspect, the object of the present invention is achieved by providing an information recording apparatus including a data record circuit responsive to a supplied control signal to record data on a mounted recording medium, an information read out circuit for reading out information from a recording medium, a first period signal detection circuit detecting a first period signal out of the read out information, a synchronizing signal generation circuit generating a plurality of synchronizing signals of different phases according to the detected first period signal, a second period signal detection circuit detecting a second period signal from the read out information, and a control circuit selectively supplying to the data record circuit as the control signal a synchronizing signal out of the plurality of synchronizing signals generated by the synchronizing signal generation circuit that has a predetermined phase difference from the second period signal detected by the second period signal detection circuit.

[0009] According to an aspect, another object of the present invention is achieved by providing a reference mark detection circuit that detects a reference mark from a recording medium in which the plane configuration of at least one sidewall of a groove for tracking is formed so that a reference mark having a relatively abrupt second waveform of an amplitude identical to that of a relatively gentle first waveform modulated by a predetermined information signal is overlapped at a constant interval on the first waveform. The reference mark detection circuit includes a circuit generating an electrical signal having a waveform corresponding to the plane configuration of the sidewall, a circuit comparing the level of the generated electrical signal with a predetermined reference level to generate a first logic signal of a first pulse having a first duration time indicating the comparison result between the first waveform and the reference level and a second pulse having a second duration time indicating the comparison result between the second waveform and the reference level, a circuit generating a second logic signal of a third pulse having a fixed third duration time in synchronization with a leading edge of each pulse of the first logic signal, and a circuit latching the logic level of the second logic signal in synchronization with a trailing edge of each pulse of the first logic signal to output the result as a detection result of a reference mark. The third duration time is longer than the second duration time and shorter than the first duration time.

[0010] According to another aspect, another object of the present invention is achieved by providing a reference mark detection circuit that detects a reference

mark from a recording medium in which the plane configuration of at least one sidewall of a groove for tracking is formed so that a reference mark having a relatively abrupt second waveform of an amplitude greater than that of a relatively gentle first waveform modulated by a predetermined information signal is overlapped at a constant interval on the first waveform. The reference mark detection circuit includes a circuit generating an electrical signal having a waveform corresponding to the plane configuration of the sidewall, a circuit comparing the level of the generated electrical signal with a first reference level that is between the peak value of the first waveform and the peak value of the second waveform to generate a first logic signal of a first pulse indicating the comparison result between the second waveform and the first reference level, a circuit comparing the level of the generated electrical signal with a second reference level that is smaller than the peak value of the first waveform to generate a second logic signal of a second pulse indicating the comparison result between the first waveform and the second reference level and a third pulse indicating the comparison result between the second waveform and the second reference level, and a circuit providing as a detection result of a reference mark a third logic signal of a fourth pulse having a leading edge in synchronization with the leading edge of the first pulse of the first logic signal and a trailing edge according to the first transition of the second logic signal subsequent to the leading edge of the first pulse.

[0011] According to a further aspect, another object of the present invention is achieved by providing a reference mark detection circuit that detects a reference mark from a recording medium in which the plane configuration of at least one sidewall of a groove for tracking is formed so that a reference mark having a relatively abrupt second waveform of an amplitude greater than that of a relatively gentle first waveform modulated by a predetermined information signal is overlapped at a constant interval on the first waveform. The reference mark detection circuit includes a circuit generating an electrical signal having a waveform corresponding to the plane configuration of the sidewall, a circuit comparing the level of the generated electrical signal with a first reference level between the peak value in the positive direction of the first waveform and the peak value in the positive direction of the second waveform to generate a first logic signal of a first pulse indicating the comparison result between the second waveform and the first reference level, a circuit comparing the level of the generated electrical signal with a second reference level that is between the peak value in the positive direction and the peak value in the negative direction of the first waveform to generate a second logic signal of a second pulse indicating the comparison result between the first waveform and the second reference level and a third pulse indicating the comparison result between the second waveform and the second reference level, a circuit comparing the level of the generated electrical signal

with a third reference level between the peak value in the negative direction of the first waveform and the peak value in the negative direction of the second waveform to generate a third logic signal of a fourth pulse indicating the comparison result between the second waveform and the third reference level, a circuit generating a fourth logic signal of a fifth pulse having a leading edge in synchronization with the leading edge of the first pulse of the first logic signal and a trailing edge according to the first transition of the second logic signal subsequent to the leading edge of the first pulse, a circuit generating a fifth logic signal of a sixth pulse having a leading edge in synchronization with the leading edge of the fourth pulse of the third logic signal and a trailing edge according to the first transition of the second logic signal subsequent to the leading edge of the fourth pulse, a circuit ANDing the fourth logic signal and the fifth logic signal, and a circuit receiving the AND to generate a pulse having a predetermined duration in synchronization with respective trailing edges of the fifth and sixth pulses to output the pulse as a detection result of a reference mark. The predetermined duration is longer than the time interval between the trailing edge of the fifth pulse and the trailing edge of the sixth pulse.

[0012] An advantage of the present invention is that data can be recorded correctly and reliably on a recording medium and data can be reproduced therefrom.

[0013] Another advantage of the present invention is that, when an address mark is formed at a groove of a recording medium together with a wobble, the address mark can be detected at high accuracy with a simple structure.

Brief Description of Drawings

[0014]

Fig. 1 is a block diagram showing an entire structure of an information reproduction apparatus according to a first embodiment of the present invention;

Fig. 2 is a plan view showing a track structure having a wobble at both sides of a groove in the optical disk of Fig. 1;

Fig. 3 is a plan view showing a track structure having a wobble formed at only one side of a groove in the optical disk of Fig. 1;

Figs. 4A and 4B are timing charts for describing an operation of the PLL circuit of Fig. 1;

Fig. 5 is a block diagram showing a structure of the delay circuit of Fig. 1;

Figs. 6A-6M are timing charts for describing an operation of the particular pattern detection circuit and switching unit of Fig. 1;

Fig. 7 is a block diagram showing a structure of an information recording/reproduction apparatus according to a second embodiment of the present invention;

Figs. 8A-8L are timing charts for describing an operation of the switching unit of Fig. 1;

Fig. 9 is a block diagram showing an entire structure of an information recording/reproduction apparatus according to a third embodiment of the present invention;

Fig. 10 is a block diagram showing a structure of the address mark detection circuit of Fig. 9;

Figs. 11A-11E are timing charts for describing an operation of the address mark detection circuit of Fig. 10;

Fig. 12 is a block diagram showing the former stage of an address mark detection circuit according to a fourth embodiment of the present invention;

Fig. 13 is a block diagram showing the latter stage of the address mark detection circuit according to the fourth embodiment of the present invention;

Figs. 14A-14K are timing charts for describing an operation of the address mark detection circuit of Figs. 12 and 13;

Figs. 15A-15K are timing charts for describing an operation of the address mark detection circuit of Figs. 12 and 13;

Fig. 16 is a block diagram showing a modification of the former stage portion of the address mark detection circuit of Fig. 12;

Fig. 17 is a block diagram showing the latter stage portion of the address mark detection circuit according to a fifth embodiment of the present invention; and

Figs. 18A-18D are timing charts for describing an operation of the address mark detection circuit of Fig. 17.

Best Mode for Carrying Out the Invention

[0015] The information reproduction apparatus, information recording apparatus, and a reference mark detection circuit according to the present invention will be described in detail with reference to the drawings.

[0016] In the drawings, the same reference characters denote the same or corresponding components.

[First Embodiment]

[0017] Fig. 1 is a block diagram showing a structure of the information reproduction apparatus according to a first embodiment of the present invention.

[0018] Figs. 2 and 3 schematically show the plane configuration of a track formed on the surface of a recording medium, for example, a magneto-optical disk. In each drawing, the region for tracking is called "groove", and the region between the grooves is called "land" hereinafter.

[0019] Fig. 2 shows the plane configuration of a magneto-optical disk in which a wobble 1 of a gentle and relatively long period is continuously formed at both sidewalls of a groove, and in which a plurality of abrupt

address marks (or fine clock mark) 2 as reference marks are formed intermittently along the track direction at a constant interval at both sidewalls. Fig. 3 shows the plane configuration of a magneto-optical disk in which a wobble 1 of a gentle and relatively long period is continuously formed at only one side of a groove, and a plurality of address marks 2 are formed intermittently along the track direction at a constant interval at both sidewalls.

[0020] In Figs. 2 and 3, the gentle waveform of wobble 1 is, as described before, modulated by a signal such as an address information signal or a synchronizing signal. At the time of recording/reproduction, the address information signal and synchronizing signal are demodulated to be used in the recording/reproduction operation. Address mark 2 having an abrupt waveform is a reference mark to indicate the beginning of data, the timing of signal recording/reproduction, and determining whether the laser beam is on the center line of the track. It is detected as a reference timing signal to which the operation will be referenced in recording/reproduction. The period of wobble 1 has a range of, for example, 10-35 μm .

[0021] As shown in Fig. 1, the information reproduction apparatus includes a spindle motor 300 for rotating an optical disk 100 at a predetermined speed of rotation, an optical head 500 directing a laser beam having a wavelength of 680 nm at a predetermined timing onto optical disk 100 to read out information such as the data and synchronizing signal recorded magnetically in advance on optical disk 100 and a wobble signal according to wobble 1 that is recorded physically, a signal reproduction amplify circuit 70 connected to optical head 500 to amplify and separate each signal of optically-reproduced data, synchronizing signal, wobble signal, and error signal, and a signal demodulation circuit 90 connected to signal reproduction amplify circuit 70 to generate in synchronization with an input clock signal reproduction data by demodulating the data amplified by signal reproduction amplify circuit 70 according to the modulated method in recording.

[0022] Further included are a servo circuit 110 receiving an error signal of a low frequency amplified and separated by signal reproduction amplify circuit 70 to rotate spindle motor 300 at a predetermined speed of rotation and also controlling the objective lens included in optical head 500 to carry out tracking servo and focus servo, a wobble detection circuit 130 connected to signal reproduction amplify circuit 70 to detect a wobble signal as a first period signal out from the amplified signal, a PLL circuit 150 connected to wobble detection circuit 130 to generate a predetermined synchronizing signal SS0 according to the wobble signal, a delay circuit 170 connected to PLL circuit 150 to generate a plurality of synchronizing signals SS0-SS10 having different phases, a particular pattern detection circuit 190 connected to signal reproduction amplify circuit 70 to detect a particular pattern as a reproduced second period signal, a switch-

ing unit 210 to selectively supply one synchronizing signal out of the plurality of synchronizing signals SS0-SS10 generated from delay circuit 170, having a predetermined phase difference from that of the particular pattern, to a laser drive circuit 230 and to a signal demodulation circuit 90, a preset circuit 180 for presetting the predetermined phase difference equal to the phase difference of recording, and a laser drive circuit 230 controlling optical head 500 so that a laser pulse beam for reproduction is directed onto optical disk 100 at a predetermined timing according to the synchronizing signal supplied from switching unit 210.

[0023] Delay circuit 170 includes ten delay elements 171-174 connected in series, as shown in Fig. 5.

[0024] The operation of the information reproduction apparatus according to the first embodiment of the present invention will be described hereinafter.

[0025] Wobble detection circuit 130 detects a wobble signal from the reproduced amplified signal. The wobble signal shown in Fig. 4A is supplied to PLL circuit 150.

[0026] PLL circuit 150 binarizes the supplied wobble signal to generate a synchronizing signal according to the binarized signal in synchronization with the timing of the binarized signal attaining a high level.

[0027] That synchronizing signal is frequency-multiplied. A synchronizing signal SS0 having a frequency 100 times that of the wobble signal is generated and output as shown in Fig. 4B.

[0028] As shown in Fig. 5, synchronizing signal SS0 is input to delay circuit 170. The synchronizing signal delayed by a predetermined time t at delay element 171 is output as synchronizing signal SS1. The synchronizing signal further delayed by time t at delay element 172 is output as synchronizing signal SS2. In a similar manner, synchronizing signals SS0-SS10 are output sequentially from delay circuit 170 to switching unit 210.

[0029] As shown in Figs. 6C-6M, time t is set as the time of, for example 1/10 the half period T1-T3 of synchronizing signal SS0.

[0030] The information as shown in Fig. 6A is magnetically recorded on optical disk 100. More specifically, data 33 and a synchronizing signal 31 indicating the beginning of data 33 are recorded in the one cycle of 2kB (170 wobbles). Also, the data (particular pattern, also called "2T pattern" hereinafter) 290 of 8 bits of (00110011) shown in Fig. 6B is recorded at two positions, i.e., the beginning of each period and during data 330.

[0031] Particular pattern detection circuit 190 detects the 2T pattern pulse signal shown in Fig. 6B that is reproduced and amplified by signal reproduction amplify circuit 70. This detected pulse signal is provided to switching unit 210.

[0032] Switching unit 210 selects one of the synchronizing signals SS0-SS10 supplied from delay circuit 170 that has the preset phase difference preset of preset circuit 180 from the 2T pattern pulse signal to provide the selected synchronizing signal to laser drive circuit 230.

[0033] For example, when a value approximating 0 is set as the phase base difference from the 2T pattern pulse signal in preset circuit 180, switching unit 210 selects one synchronizing signal SS3 that attains a high level at a time closest to time T2 where the 2T pattern pulse signal of Fig. 6B first attains a high level.

[0034] As a result of signal demodulation circuit 90 establishing synchronization by this selected one synchronizing signal SS3, the signal reproduced and amplified by signal reproduction amplify circuit 70 is demodulated to result in reproduction data.

[0035] This one selected synchronizing signal SS3 is provided to laser drive circuit 230, whereby optical head 500 projects a laser beam that is pulsed in synchronization with synchronizing signal SS3 to optical disk 100.

[0036] 2T pattern 290 is also inserted in data 330 to supply a predetermined synchronizing signal reliably to laser drive circuit 230 and signal demodulation circuit 90. The desired synchronizing signal is reselected (selection is reevaluated) during one period.

[0037] According to the information reproduction apparatus of the first embodiment, error in data reproduction can be reduced by establishing the optimum timing for data reproduction with respect to the data recorded magnetically.

[0038] Also, information of high density can be reproduced accurately by preventing the drop of reproduction data to carry out reproduction properly.

[0039] The information reproduction apparatus according to the first embodiment of the present invention is premised on the magnetic recording of a particular pattern (2T pattern) 290 on a mounted optical disk 100 from which one synchronizing signal having a predetermined phase difference is selected by switching unit 210 with the reference of the 2T pattern 290 in the reproduction of optical disk 100. Alternatively, an information reproduction apparatus that detects a fine clock mark 2 physically recorded as shown in Figs. 2 and 3 instead of 2T pattern 290 to select one synchronizing signal having a predetermined phase difference with the detected signal as the reference by switching unit 210 is similarly applicable.

[Second Embodiment]

[0040] Fig. 7 is a block diagram showing a structure of an information recording/reproduction apparatus according to a second embodiment of the present invention.

[0041] As shown in Fig. 7, the information recording/reproduction apparatus includes a signal modulation circuit 290 modulating the recorded data at a predetermined modulation system such as the 1-7 system, a write timing generation circuit 310 connected to signal modulation circuit 290 and a switching unit 210, generating a magnetic head drive signal to establish timing of writing data into optical disk 100 according to the signal modulated by signal modulation circuit 290

and the synchronizing signal from switching unit 210, a magnetic head 350 applying a magnetic field to optical disk 100, and a magnetic head drive circuit 330 driving magnetic head 350 so as to apply a magnetic field in a direction determined by a magnetic head drive signal.

[0042] Further included are a spindle motor 300 to rotate optical disk 100 at a predetermined speed of rotation, an optical head 500 directing a laser pulse beam having a wavelength of 680 nm at a predetermined timing on optical disk 100 to magnetically record data and the like onto optical disk 100 and also reading out information such as the data and synchronizing signal recorded magnetically, a wobble signal, a fine clock signal, or the like according to physically recorded wobble 1 and fine clock mark 2, a signal reproduction amplify circuit 70 connected to optical head 500 for amplifying and separating each of the signals of the data, synchronizing signal, wobble signal, fine clock signal, and error signal optically-reproduced, and a servo circuit 110 receiving an error signal of low frequency amplified and separated by signal reproduction amplify circuit 70 to rotate spindle motor 300 at a predetermined speed of rotation, and also controlling the objective lens included in optical head 500 so as to carry out tracking servo control and focus servo control.

[0043] Further included are a wobble detection circuit 130 connected to signal reproduction amplify circuit 70 to detect a wobble signal as a first period signal out of the amplified signal, a PLL circuit 150 connected to wobble detection circuit 130 to generate a predetermined synchronizing signal SS0 according to the wobble signal, a delay circuit 170 connected to PLL circuit 150 to generate a plurality of synchronizing signals SS0-SS10 of different phases, a fine clock mark detection circuit 190 connected to signal reproduction amplify circuit 70 to detect a fine clock signal as a reproduced second synchronizing signal, a switching unit 210 selectively providing to a write timing generation circuit 310 and a laser drive circuit 230 a synchronizing signal out of the plurality of synchronizing signals SS0-SS10 generated from delay circuit 170 that has a predetermined phase difference from the fine clock signal, a preset circuit 180 for presetting the predetermined phase difference, and a laser drive circuit 230 for controlling optical head 500 so that a laser pulse beam is directed to optical disk 100 at a predetermined timing according to the synchronizing signal supplied from switching unit 210 in data recording and reproduction.

[0044] The recording operation of the above information recording/reproduction apparatus according to the second embodiment of the present invention will be described hereinafter.

[0045] This operation is similar to the operation of the information reproduction apparatus of the first embodiment, provided that fine clock mark detection circuit 190 detects the fine clock signal from the signal reproduced and amplified by signal reproduction amplify circuit 70 and provides to switching unit 210 the fine clock sig-

nal taking a high (H) level for a predetermined time shown in Fig. 8A.

[0046] Switching unit 210 selects one synchronizing signal that attains a high level the preset time (phase) of preset circuit 180 behind time T2 where the fine clock signal of Fig. 8A attains a high level, and supplies the selected synchronizing signal to write timing generation circuit 310 and laser drive circuit 230.

[0047] When the value is set as a phase difference approximating 0 at preset circuit 180, synchronizing signal SS3 of Fig. 8E that attains a high level at the time closest to time T2 is selected by switching unit 210. The same synchronizing signal SS3 is supplied to write timing generation circuit 310 and laser drive circuit 230.

[0048] By driving magnetic head 350 and optical head 500 with the same synchronizing signal, a laser pulse beam can be directed at a desired timing when a predetermined magnetic field is applied to optical disk 100. Thus, data can be recorded at high density appropriately.

[0049] The reproduction operation of the information recording/reproduction apparatus according to the second embodiment of the present invention will be described hereinafter.

[0050] This operation is similar to the reproduction operation of the information reproduction apparatus of the first embodiment, provided that fine clock mark detection circuit 190 detects a fine clock signal from the signals reproduced and amplified by signal reproduction amplify circuit 70 to supply a fine clock signal having a high level for a predetermined time to switching unit 210.

[0051] Switching unit 210 selects one (in the above example, synchronizing signal SS3 is selected) of synchronizing signals SS0-SS10 having a phase difference set by preset circuit 280 in recording with respect to the fine clock signal. The selected signal is supplied to laser drive circuit 230.

[0052] Laser drive circuit 230 responds to the supplied synchronizing signal to drive optical head 500 so as to emit a laser pulse beam at a predetermined timing to optical disk 100.

[0053] The optically reproduced data and the like are applied to signal reproduction amplify circuit 70 to be amplified. The amplified signal is demodulated according to the modulation system of signal modulation circuit 290 in recording, whereby reproduction data is generated (demodulation circuit is not depicted).

[0054] According to the information recording/reproduction apparatus of the second embodiment of the present invention, data is recorded taking advantage of a synchronizing signal having a predetermined phase difference on the basis of a fine clock mark 2 that is physically recorded on optical disk 100. Therefore, recording of equal quality can be reliably carried out. Furthermore, since the recorded data is reproduced using a synchronizing signal having the predetermined phase difference used in recording, a more accurate

and reliable reproduction data can be obtained.

[Third Embodiment]

[0055] Although the formation of an address mark (or fine clock mark) at the groove on recording medium in addition to a wobble is conventionally proposed, a circuit that detects such an address mark accurately with the simple structure has not yet been proposed.

[0056] In the following embodiment, a reference mark detection circuit that detects particularly an address mark accurately will be described in detail.

[0057] Fig. 9 is a block diagram showing an entire structure of an information recording/reproduction apparatus including a reference mark (address mark or fine clock mark) detection circuit to detect address mark 2 shown in Figs. 2 and 3.

[0058] First, the entire structure of an information recording/reproduction apparatus of a magneto-optical disk according to a third embodiment of the present invention will be described with reference to Fig. 9.

[0059] Referring to Fig. 9, the information recording/reproduction apparatus includes a signal modulation circuit 11, a timing pulse generation circuit 12, a magnetic head drive circuit 13, a laser drive circuit 14, an optical head 15, a magnetic head 16, a spindle motor 17, a servo circuit 18, a reproduced signal amplify circuit 19, a low pass circuit 20, a clock generation circuit 21, a decoder 22, an address mark detection circuit 23, a synchronizing signal input circuit 24, and a duty correction circuit 25.

[0060] First, the recording operation of the information recording/reproduction apparatus of Fig. 9 will be described. The record data indicating the information to be recorded is sent to signal modulation circuit 11 to be modulated by, for example, the 1-7 RLL system. Following the modulation of the 1-7 RLL system, the data is sent to timing pulse generation circuit 12 to be modified into a pulse signal having a predetermined duty ratio. Also, the predetermined phase difference is set. Then, the pulse signal is sent to magnetic head drive circuit 13 and laser drive circuit 14.

[0061] Laser drive circuit 14 turns on/off the semiconductor laser (not shown) in optical head 15 in response to the sent pulse signal. As a result, a pulsed laser beam is directed on magnet-optical disk 26. Magnetic head drive circuit 13 responds to the applied record signal to drive magnetic head 16, whereby the record signal is recorded on magneto-optical disk 26.

[0062] In the present embodiment, the phase of the pulse laser beam is behind the phase of the record magnetic field by 0-60 ns. The duty ratio of the pulse laser beam is 20-60%. The information to be recorded is not limited to the above video signal, and may be an audio signal, a data signal, and the like.

[0063] The reproduction operation of the information recording/reproduction apparatus of Fig. 9 will be described hereinafter.

[0064] A laser beam is emitted from the semiconductor laser (not shown) of optical head 15. The beam passes through an objective lens (not shown) in optical head 15 to be directed on the recording plane of magneto-optical disk 26. The light reflected from the recording plane is detected by a photodetector (not shown) in head 15, whereby a reproduced signal is output from optical head 15.

[0065] The obtained reproduced signal is sent to reproduced signal amplify circuit 19 to be amplified. The amplified signal is sent to low pass circuit 20. The reproduced signal passing through low pass circuit 20 is sent to decoder 22 to be demodulated by the 1-7 system in synchronization with the clock signal sent from clock generation circuit 21 to be output as reproduction data.

[0066] The reproduced signal is amplified by reproduced signal amplify circuit 19 and sent to servo circuit 18. Servo circuit 18 controls optical head 15 and spindle motor 17, whereby data is read out from magneto-optical disk 26.

[0067] The reproduced data amplified by reproduced signal amplify circuit 19 is also applied to address mark detection circuit 23 of the present invention. Address mark detection circuit 23 detects the address mark formed at the groove of the magneto-optical disk shown in Fig. 2 or 3 to generate a reference timing signal. Synchronizing signal input circuit 24 generates a synchronizing signal to direct a laser beam onto disk 26 according to the reference timing signal from address mark detection circuit 23. The generated synchronizing signal is applied to duty correction circuit 25.

[0068] Duty correction circuit 25 generates a pulse signal of a predetermined duty according to the synchronizing signal from synchronizing signal input circuit 24. The generated pulse signal is applied to laser drive circuit 14. Laser drive circuit 14 controls optical head 15 according to the pulse signal from duty correction circuit 25, whereby the reproduction laser beam is pulsed. The output pulse signal from duty correction circuit 25 may be applied to signal modulation circuit 11 as the trigger of signal modulation.

[0069] Fig. 10 is a block diagram showing the structure of address mark detection circuit 23 out of the entire structure of the information recording/reproduction apparatus of Fig. 9. In the third embodiment, an address mark detection signal that is particularly formed to correspond to a magneto-optical disk in which the amplitude of the wobble is identical to the amplitude of the address mark will be described in detail.

[0070] Referring to Fig. 10, the reproduced signal output from reproduced signal amplify circuit 19 of Fig. 9 is applied to amplifier 32 via high pass filter 31 to be amplified. The output from amplifier 32 is applied to one fixed terminal of switch circuit 34 and also to the other fixed terminal of switch circuit 34 via an inversion amplifier 33. The movable terminal of switch circuit 34 is applied to the positive input terminal of comparator 35. The switching control of switch circuit 34 is effected by a control

signal from a control circuit not shown.

[0071] The negative input terminal of a comparator 35 is connected to the ground potential. The output of comparator 35 is applied to a one shot circuit 36. The output of one shot circuit 36 is applied to the data input of a flip-flop circuit 37. The inverted output of comparator 35 is applied to the clock input of flip-flop circuit 37. Flip-flop circuit 37 outputs a reference timing signal, which is applied to synchronizing signal input circuit 24 of Fig. 9.

[0072] Figs. 11A-11E are timing charts for describing the operation of the address mark detection circuit of Fig. 10. The operation of the address mark detection circuit according to the third embodiment of the present invention will be described hereinafter with reference to Figs. 10 and 11A-11E.

[0073] First, the output of amplifier 32 is applied to the positive input of comparator 35 by switch circuit 34. The waveform at the positive input of comparator 35 is represented in Fig. 11A. This signal is a reproduced electrical signal having a waveform corresponding to the plane configuration of the groove of magneto-optical disk 26. This waveform includes a relatively gentle wobble 1 and an abrupt address mark 2 formed thereon at a predetermined interval.

[0074] It is assumed that address mark 2 always has the shape as shown in Fig. 11A in the embodiment set forth in the following. However, the waveform of this address mark 2 may be inverted depending upon the disk. In such a case, the waveform of the address mark at the positive input of comparator 35 is maintained at the shape shown in Fig. 11A by providing the output via inversion amplifier 33 to the positive input of comparator 35 by controlling switch circuit 34 by a control circuit not shown.

[0075] The waveform (Fig. 11A) applied to the positive input of comparator 35 is compared with the reference level (here, ground level) applied to the negative input. The comparison result (Fig. 1B) is applied to one shot circuit 36. One shot circuit 36 generates a pulse having a constant duration t (Fig. 11C) in synchronization with the rise of the output (Fig. 11B) of comparator 35. The generated pulse is applied to the data input of flip-flop circuit 37.

[0076] The inverted output (Fig. 11D) of comparator 35 is applied to the clock input of flip-flop circuit 37. Flip-flop circuit 37 maintains the level of the data input (Fig. 11C) for every rise (arrow) of the clock input (Fig. 11D) to output the maintained level as the reference timing signal (Fig. 11E).

[0077] As to the output of comparator 35, t is preset so that the relationship of $t_1 < t < t_2$ is established where t_2 is the duration of the pulse indicating the comparison result between a portion 1 of the wobble and the reference level (ground potential), t_1 is the duration of the pulse indicating the comparison result between the portion of address mark 2 and the reference level, and t is the duration of the output pulse of one shot circuit 36.

[0078] When a pulse of a duration t_2 indicating the

comparison result with wobble 1 is generated at the output (Fig. 11B), an L level is always detected at the rise of the clock input (Fig. 11D) since duration t of the one shot pulse of the signal (Fig. 11C) is shorter than t_2 . However, when a pulse of a duration t_1 corresponding to address mark 2 is generated at the output (Fig. 11B), an H level is detected at the rise of the clock input (Fig. 11D) of flip-flop circuit 37 since a one shot pulse of a duration t longer than duration t_1 is generated. The detected H level continues until an L level is detected at the timing corresponding to the trailing edge of the next detected pulse of wobble 1.

[0079] Thus, the detection pulse is generated at the output of flip-flop circuit 37 only when a signal corresponding to address mark 2 of duration t_1 is detected.

[0080] According to the third embodiment of the present invention, the gentle waveform of the wobble is not detected and only the abrupt waveform change of the address mark is detected to generate a reference timing signal properly in the case where a signal is to be reproduced from a magneto-optical disk in which the wobble and the address mark are formed having the same amplitude.

[Fourth Embodiment]

[0081] The fourth embodiment of the present invention relates to an address mark detection circuit that is formed to correspond to a magneto-optical disk in which an address mark is formed having an amplitude greater than the amplitude of the wobble.

[0082] Figs. 12 and 13 are block diagrams showing a structure of the former stage portion and later stage portion, respectively, of such an address mark detection circuit.

[0083] Referring to Fig. 12, the reproduced signal from reproduced signal amplify circuit 19 of Fig. 10 is applied to amplifier 47 via a high pass filter 41 to be amplified. The output of amplifier 42 is applied in common to the positive input of comparators 43, 44, and 45.

[0084] A positive reference potential A is applied to the negative input of comparator 43. A negative reference potential C is applied to the negative input of comparator 44. A ground potential B is applied to the negative input of comparator 45.

[0085] The output of comparator 43 is applied to a reset input 52 of a flip-flop circuit 47 via an inverter 46. The output of comparator 44 is applied to a reset input 53 of flip-flop circuit 49. The output of comparator 45 is applied to the clock input terminal of flip-flop circuit 49 as well as to the clock input terminal of flip-flop circuit 47 via inverter 48.

[0086] The outputs of flip-flop circuits 47 and 49 are ANDed by an AND gate 50. The output of AND gate 50 is applied to one shot circuit 51. The output of one shot circuit 51 is output from address mark detection circuit 23 as a reference timing signal to be applied to synchronizing signal input circuit 24 of Fig. 9.

[0087] Figs. 14A-14K and 15A-15K are timing charts for describing the operation of the address mark detection circuit of Figs. 12 and 13. The operation represented by Figs. 14A-14K differs from the operation represented by Figs. 15A-15K in that the phase of the waveform of address mark 2 is inverted.

[0088] The operation of address mark detection circuit 23 in the case where an address mark having the waveform of Fig. 14A is detected will be described first.

[0089] An electrical signal having a waveform corresponding to the plane configuration of the groove as shown in Fig. 14A is output from amplifier 42 of Fig. 12 to be applied to the positive input of comparators 43-45. A potential corresponding to a reference level A greater than the peak value of wobble 1 and smaller than the peak value of address mark 2, as shown in A in Fig. 14A, is applied to the negative input of comparator 43. A signal (Fig. 14B) including a pulse corresponding to the comparison result between the waveform of Fig. 14A and reference level A is output from comparator 43. This signal (Fig. 14B) is inverted by inverter 46 and then applied to reset input 52 of flip-flop circuit 47.

[0090] A potential corresponding to a reference level C greater than the peak value in the negative direction of wobble 1 and smaller than the peak value in the negative direction of address mark 2, as shown in C in Fig. 14A, is applied to the negative input of comparator 44. A signal (Fig. 14G) including a pulse indicating the comparison result between the waveform of Fig. 14A and reference level C is output from comparator 44 to be applied to the reset input 53 of flip-flop circuit 49.

[0091] The ground potential B of Fig. 14A is applied to the negative input of comparator 45. A signal (Fig. 14D) including a pulse indicating the comparison result between the waveform of Fig. 14A and ground potential B is output from comparator 45. This signal (Fig. 14D) is applied to the clock input of flip-flop circuit 49, and also inverted by inverter 48 to be applied to the clock input of flip-flop circuit 47. It is assumed that the data input of flip-flop circuits 47 and 49 is connected to the potential of an H level.

[0092] Referring to Figs. 14A-14K, when the amplitude in the positive direction of address mark 2 is detected by comparator 43 as the signal represented by Fig. 14B, flip-flop circuit 47 is reset by this inverted signal (Fig. 14C). The output (Fig. 14F) is driven from the H level to an L level. Then, flip-flop circuit 47 retains the H level of the data input at the rising (arrow) timing of the signal (Fig. 14E) which is the clock input to maintain the output (Fig. 14F) at the H level until the next reset pulse is input. In other words, a one shot pulse waveform of Fig. 14F is obtained corresponding to the amplitude in the positive direction of the address mark.

[0093] The waveform of the address mark in the negative direction is detected as the pulse (Fig. 14G) by comparator 44. Flip-flop circuit 49 is reset by this pulse (Fig. 14G), whereby the output (Fig. 14I) is driven from the H level to an L level. Then, flip-flop circuit 49 retains

the data input of an H level in synchronization with the rising (arrow) timing of the signal (Fig. 14D) which is the clock input. The signal of Fig. 14I is maintained at the H level until the next reset pulse is input. In other words, a one shot pulse of Fig. 14I is detected according to the amplitude of the address mark in the negative direction. When the waveform of address mark 2 is always constant as shown in, for example, Fig. 14A, the detection of an address mark is effected by detecting either this pulse signal (Fig. 14F) or the pulse signal (Fig. 14I).

[0094] However, since there may be a case where the phase of the address mark is inverted as will be described afterwards in connection with Figs. 15A-15K, these signals (Fig. 14F) and the signal (Fig. 14I) are ANDed (Fig. 14J) by AND gate 50 to generate a detection signal according to the result in the present fourth embodiment.

[0095] More specifically, by applying a signal (Fig. 14J) to one shot signal 51 that generates a pulse of a duration longer than the time interval of respective trailing edges of two continuous pulses that are output (Fig. 14J) from AND gate 50, a signal (Fig. 14K) including a one shot pulse indicating the detection of an address mark can be obtained.

[0096] The operation of detecting an address mark 2 having an inverted waveform will be described with reference to Figs. 15A-15K. The waveforms of Figs. 15B, 15D and 15G are obtained from comparators 43, 44, and 45, respectively, of Fig. 12. Flip-flop circuit 47 is reset by a reset pulse (Fig. 15C) to latch the data of an H level at the rising (arrow) timing of the clock input (Fig. 15E). The pulse (Fig. 15F) is output from flip-flop circuit 47 to be applied to one input of AND gate 50.

[0097] Flip-flop circuit 49 is reset by a reset pulse (Fig. 15G) to retain the data of the H level at the rising (arrow) timing of the clock input (Fig. 15D). Therefore, the pulse (Fig. 15I) is output from flip-flop circuit 49 to be applied to the other input of AND gate 50.

[0098] As a result, a signal representing the AND (Fig. 15J) is obtained from AND circuit 50. This signal is applied to one shot circuit 51, whereby a pulse (Fig. 15K) having a duration longer than the time interval of the trailing edge of the two pulses of the signal (Fig. 15J) is generated from circuit 51. This pulse (Fig. 15K) is output as the signal indicating detection of an address mark.

[0099] According to the fourth embodiment of the present invention, an address mark can be detected reliably independent of the phase of the waveform of the address mark when the amplitude of the address mark is greater than that of the wobble.

[0100] Comparators 43 and 44 of Fig. 12 can be used in common with one comparator by providing an inversion circuit 54 and a switch 55 as shown in Fig. 16 to switch the polarity towards the positive input of the comparator. Accordingly, the circuit configuration can be made more simple.

[Fifth Embodiment]

[0101] Fig. 17 is a block diagram showing the structure of the latter stage of the address mark detection circuit according to a fifth embodiment of the present invention. The former stage portion is as shown in Fig. 12 or 16. The embodiment shown in Fig. 17 is directed to realize a detection circuit that will not detect a scratch erroneously as an address mark even when, for example, there is such a scratch between the address marks on the surface of a disk. The structure of the detection circuit differs from the structure of the fourth embodiment shown in Fig. 13 in that an OR gate 56 is provided to feed back the output of one shot circuit 51 to its input. [0102] Figs. 18A-18D are timing charts to describe the operation of the address mark detection circuit of Fig. 17.

[0103] Referring to Figs. 17 and 18A-18D, when there is a physical scratch 3 in the groove between two address marks as shown in Fig. 18A, a pulse corresponding to this scratch is detected by flip-flop circuits 47 and 49. A pulse corresponding to the AND thereof is output from AND gate 50 (Fig. 18B). Here, the duration of the pulse generated by one shot circuit 51 is set longer than the duration t_1 of respective trailing edges ((a) and (b) of Fig. 18B) of the pulse corresponding to the amplitudes in the positive direction and the negative direction of the address mark in the previous fourth embodiment, and shorter than the duration t_2 starting from the position of elapse (b) of t_1 up to the trailing edge (d) of the pulse corresponding to the amplitude in the positive direction of the next address mark. By ORing that pulse and the output (Fig. 18B) of AND gate 50 by use of an OR gate 56, the pulse corresponding to scratch 3 will not be erroneously detected as a detection pulse of the address mark.

[0104] Preferably, the duration is set to a time interval close to time interval t_2 . Also, the duration time ($t_1 < t < t_2$) under control of one shot circuit 51 can have the clock counted with a digital counter to set the time close to the time of ($t_1 + t_2$) of Fig. 18B.

[0105] According to the present fifth embodiment, the timing of an address mark can be detected correctly without being influenced by a scratch, if any, between the address marks on the surface of the disk.

Claims

1. An information reproduction apparatus comprising:

information read out means (230, 500) responsive to a supplied control signal for reading out information from a mounted recording medium, reproduction means (90) for demodulating said information to generate reproduction data, first period signal detection means (130) for detecting a first period signal from read out said information,

synchronizing signal generation means (170) for generating a plurality of synchronizing signals of different phases according to detected said first period signal,

second period signal detection means (190) for detecting a second period signal from read out said information, and

control means (210) for selectively supplying as said control signal to said information read out means a synchronizing signal out of said plurality of synchronizing signals generated by said synchronizing signal generation means that has a predetermined phase difference from said second period signal detected by said second period signal detection means.

2. An information recording apparatus comprising:

data record means (310, 330, 350) for recording data to a mounted recording medium in response to a supplied control signal, information read out means (230, 500) for reading out information from said recording medium,

first period signal detection means (130) for detecting a first period signal from read out said information,

synchronizing signal generation means (170) for generating a plurality of synchronizing signals of different phases according to detected said first period signal,

second period signal detection means (190) for detecting a second period signal from read out said information, and

control means (210) for selectively supplying as said control signal to said data record means a synchronizing signal out of said plurality of synchronizing signals generated by said synchronizing signal generation means that has a predetermined phase difference from said second period signal detected by said second period signal detection means.

3. A reference mark detection circuit for detecting a reference mark from a recording medium in which the plane configuration of at least one sidewall of a groove for tracking is formed so that said reference mark having, on a relatively gentle first waveform modulated by a predetermined information signal, a relatively abrupt second waveform is overlapped at a constant interval, said first waveform and said second waveform having the same amplitude, said reference mark detection circuit comprising:

means (32) for generating an electrical signal having a waveform corresponding to said plane configuration of the sidewall, means (35) for comparing a level of said gener-

ated electrical signal with a predetermined reference level to generate a first logic signal of a first pulse having a first duration indicating the comparison result between said first waveform and said reference level and a second pulse

means (36) for generating a second logic signal of a third pulse having a fixed third duration in synchronization with a leading edge of each pulse of said first logic signal, and means (37) for latching a logic level of said second logic signal in synchronization with a trailing edge of each pulse of said first logic signal to provide the result as a detection result of said reference mark,

wherein said third duration is longer than said second duration and shorter than said first duration.

4. A reference mark detection circuit for detecting a reference mark from a recording medium in which the plane configuration of at least one sidewall of a groove for tracking is formed so that said reference mark having, on a relatively gentle first waveform modulated by a predetermined information signal, a relatively abrupt second waveform is overlapped at a constant interval, said second waveform having an amplitude greater than the amplitude of said first waveform, said reference mark detection circuit comprising:

means (42) for generating an electrical signal having a waveform corresponding to said plane configuration of the sidewall, means (43) for comparing a level of said generated electrical signal with a first reference level between a peak value of said first waveform and a peak value of said second waveform to generate a first logic signal of a first pulse indicating the comparison result between said second waveform and said first reference level, means (45) for comparing a level of said generated electrical signal with a second reference level lower than the peak value of said first waveform to generate a second logic signal of a second pulse indicating the comparison result between said first waveform and said second reference level and a third pulse indicating the comparison result between said second waveform and said second reference level, and

means (46-51) for providing as a detection result of said reference mark a third logic signal of a fourth pulse having a leading edge in synchronization with the leading edge of said first pulse of said first logic signal and a trailing

edge according to a first transition of said second logic signal subsequent to a leading edge of said first pulse.

5. A reference mark detection circuit for detecting a reference mark from a recording medium in which the plane configuration of at least one sidewall of a groove for tracking is formed so that said reference mark having, on a relatively gentle first waveform modulated by a predetermined information signal, a relatively abrupt second waveform is overlapped at a constant interval, said second waveform having an amplitude greater than the amplitude of said first waveform, said reference mark detection circuit comprising:

means (42) for generating an electrical signal having a waveform corresponding to said plane configuration of the sidewall,

means (43) for comparing a level of said generated electrical signal with a first reference level between a peak value of said first waveform in a positive direction and a peak value of said second waveform in the positive direction to generate a first logic signal of a first pulse indicating the comparison result between said second waveform and said first reference level,

means (45) for comparing the level of said generated electrical signal with a second reference level between peak values of said first waveform in a positive direction and a negative direction to generate a second logic signal of a second pulse indicating the comparison result between said first waveform and said second reference level, means (44) for comparing the level of said generated electrical signal with a third reference level between the peak value of said first waveform in the negative direction and the peak value of said second waveform in the negative direction to generate a third logic signal of a fourth pulse indicating the comparison result between said second waveform and said third reference level,

means (47) for generating a fourth logic signal of a fifth pulse having a leading edge in synchronization with the leading edge of said first pulse of said first logic signal and a trailing edge according to a first transition of said second logic signal subsequent to the leading edge of said first pulse,

means (49) for generating a fifth logic signal of a sixth pulse having a leading edge in synchronization with the leading edge of said fourth pulse of said third logic signal and a trailing edge according to a first transition of said sec-

ond logic signal subsequent to the leading edge of said fourth pulse,

means (50) for ANDing said fourth logic signal and said fifth logic signal, and

means (51) receiving said AND for generating 5
a pulse having a predetermined duration to provide the generated pulse as a detection result of said reference mark, in synchroniza-
tion with respective trailing edges of said fifth 10
and sixth pulses, said predetermined duration longer than a time interval between the trailing edge of said fifth pulse and the trailing edge of said sixth pulse.

6. The reference mark detection circuit according to 15
claim 5, wherein said predetermined duration is shorter than the time interval starting from the trailing edge of a latter one of said fifth and sixth pulses up to the trailing edge of a leading one of said fifth and sixth pulses, and 20

OR means (56) for ORing said AND and said pulse having the predetermined duration to supply said OR to said means for generating a pulse having the predetermined duration.

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FIG. 1

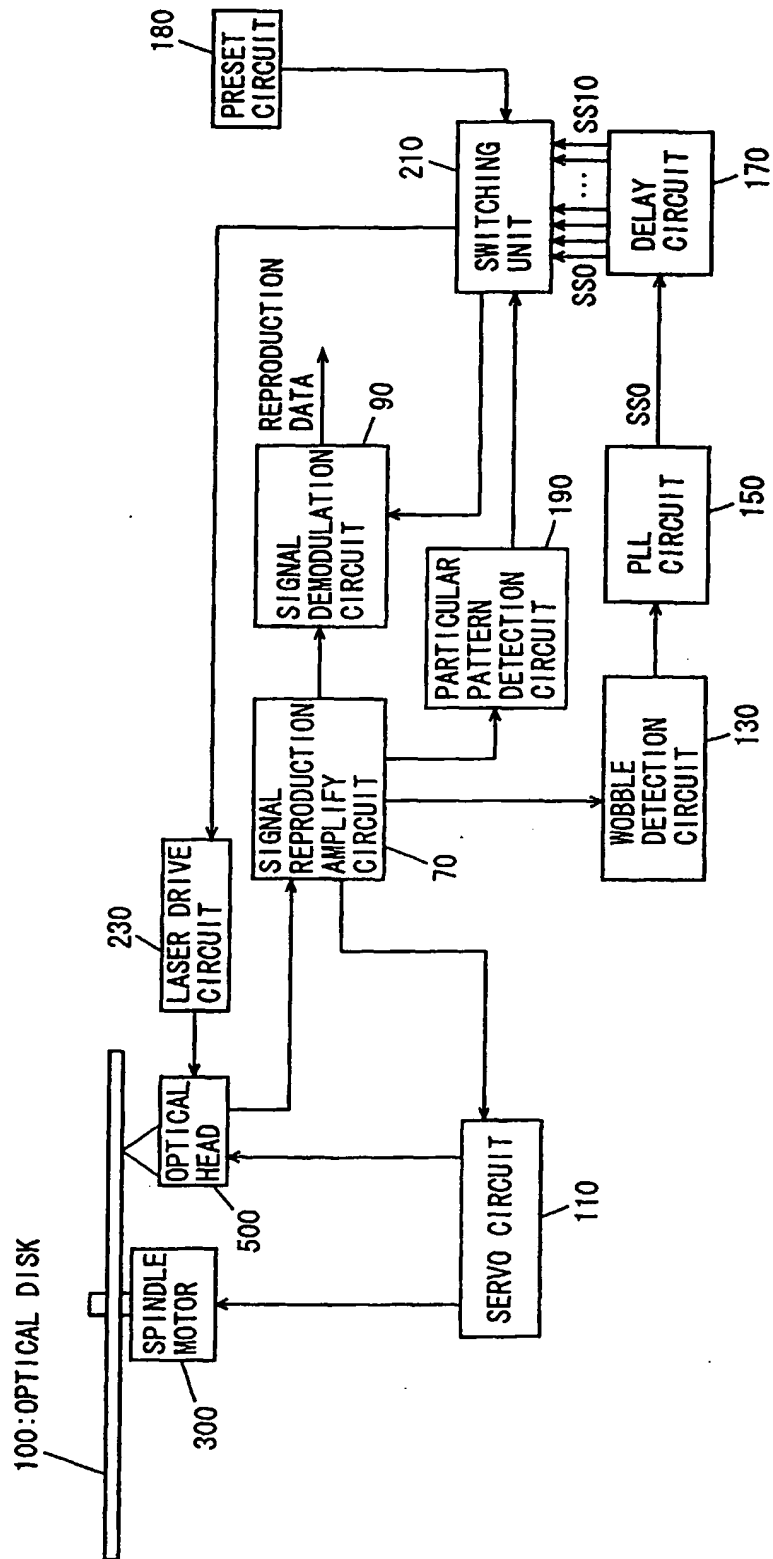


FIG. 2

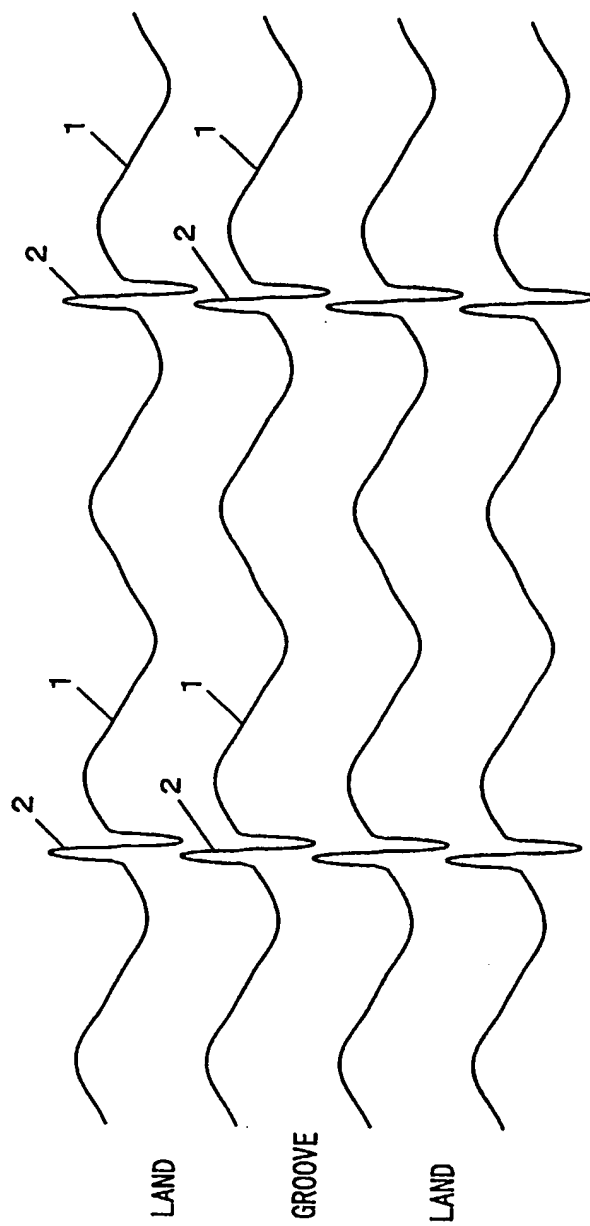


FIG. 3

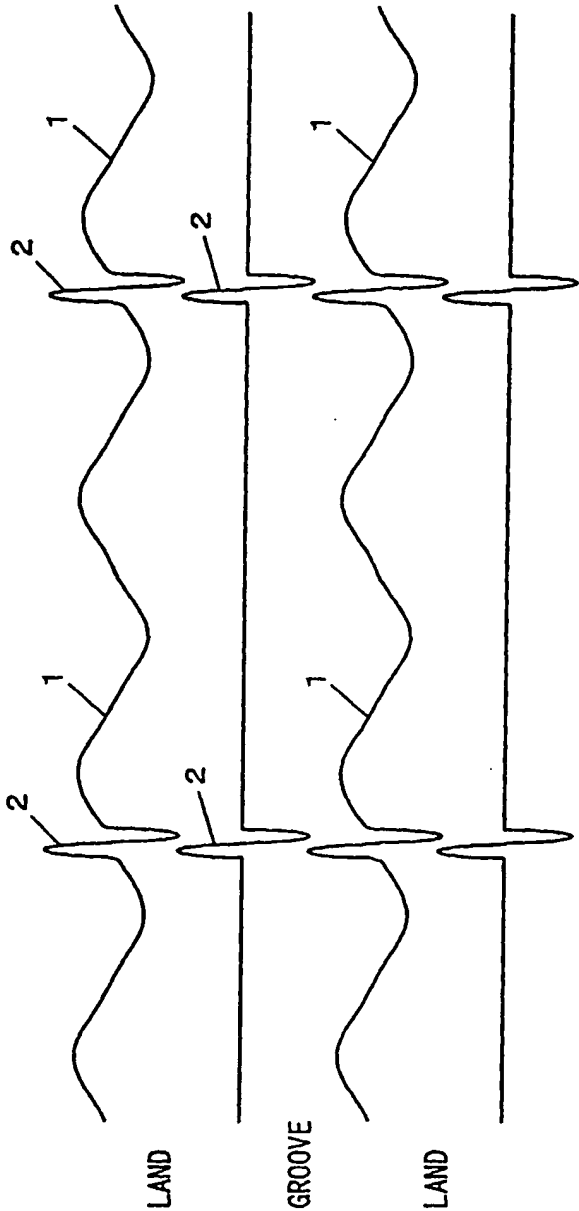


FIG. 4A

WOBBLE SIGNAL

FIG. 4B

SS0

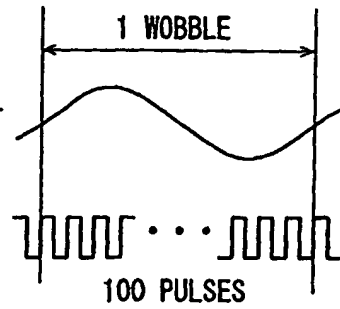
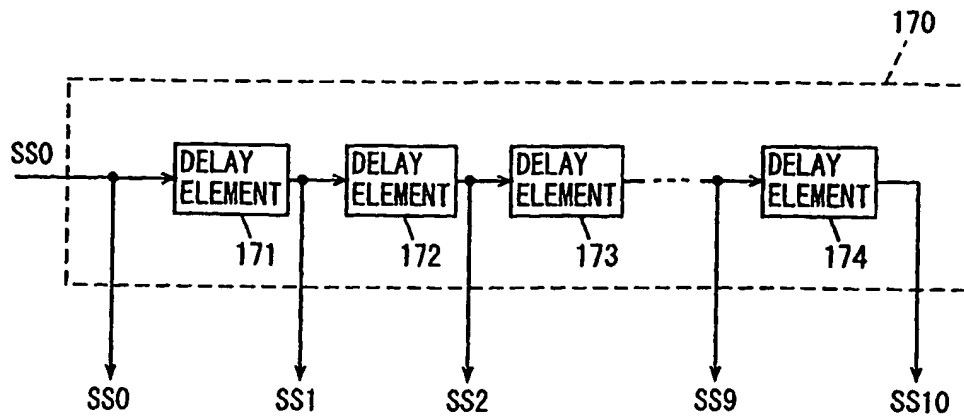


FIG. 5



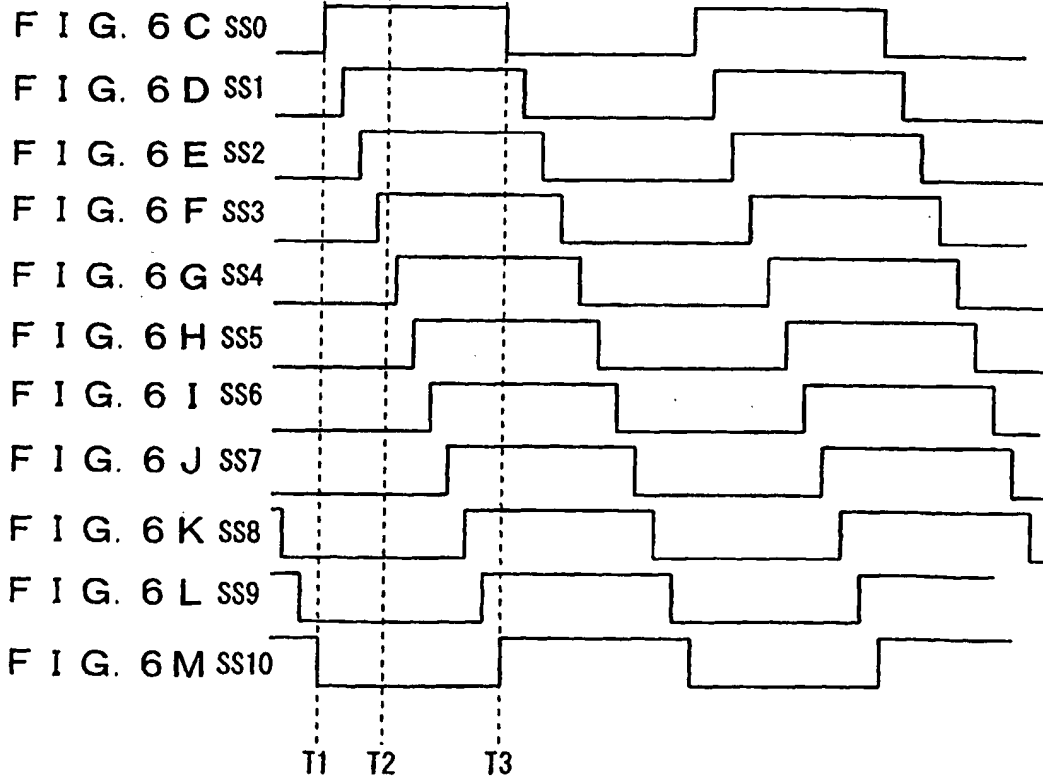
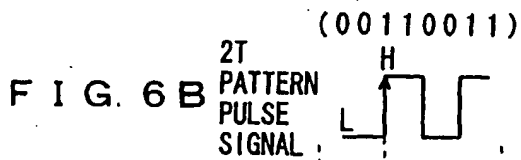
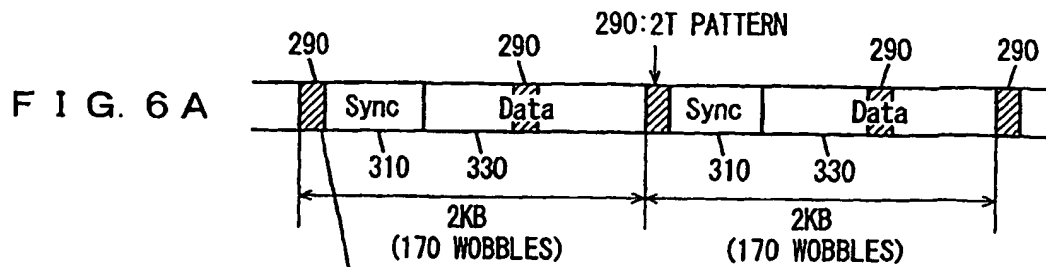
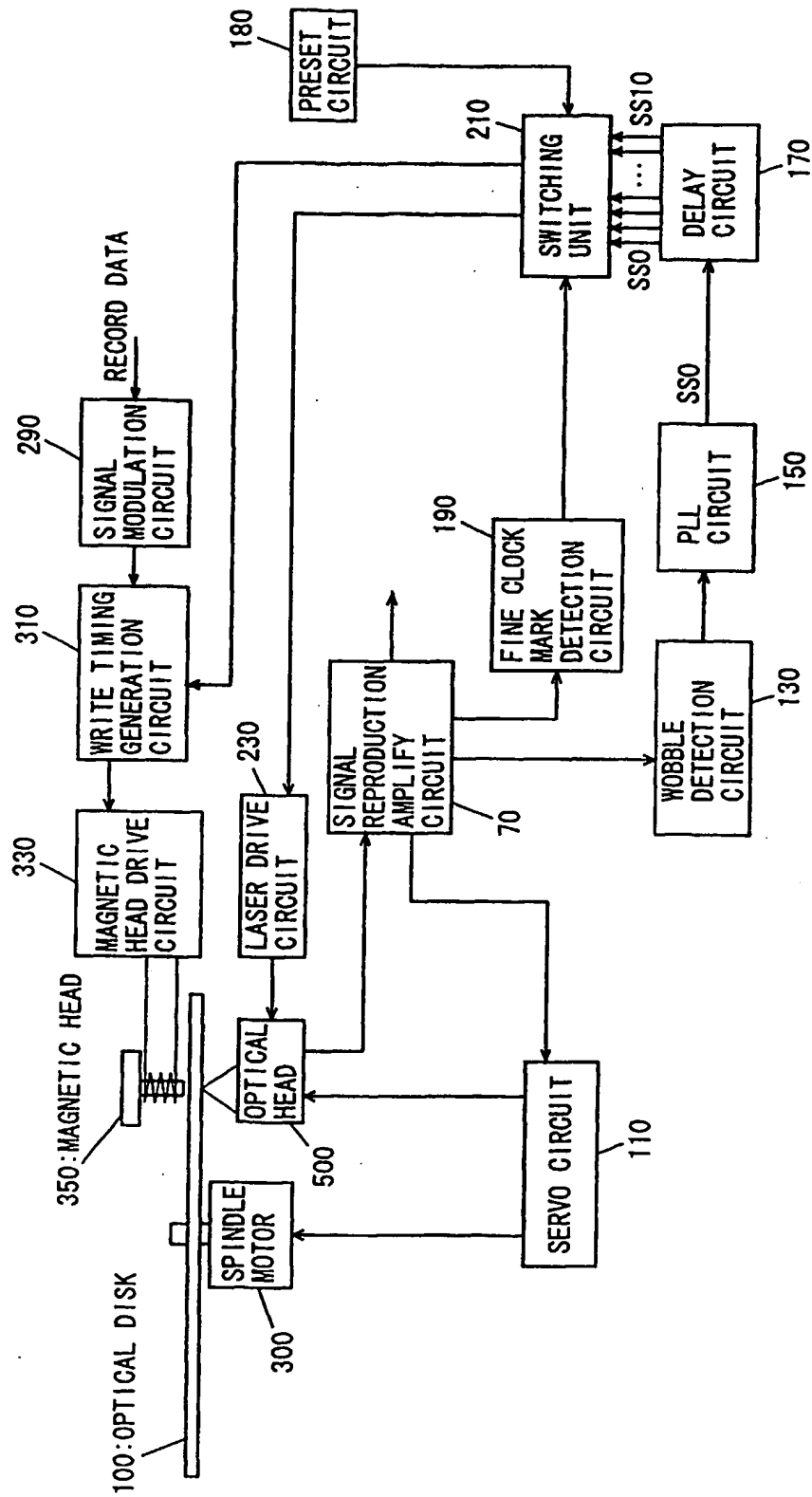


FIG. 7



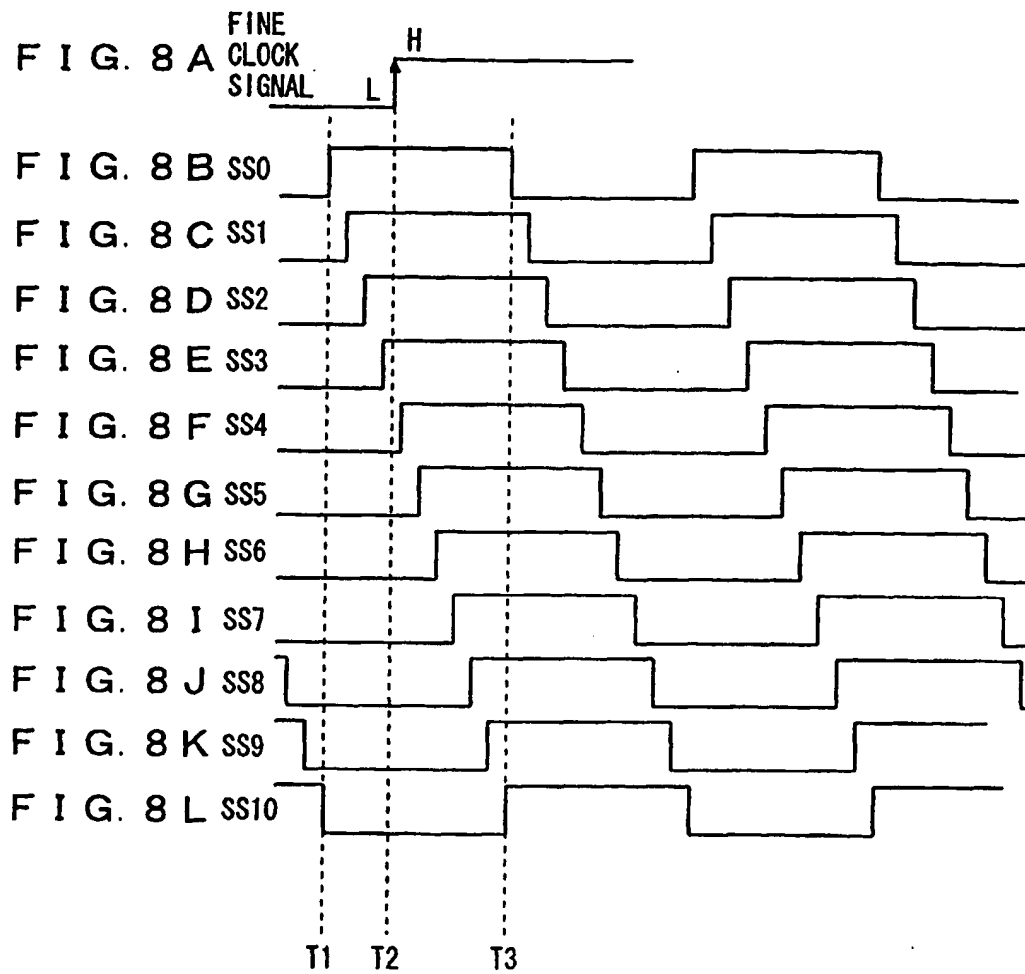


FIG. 9

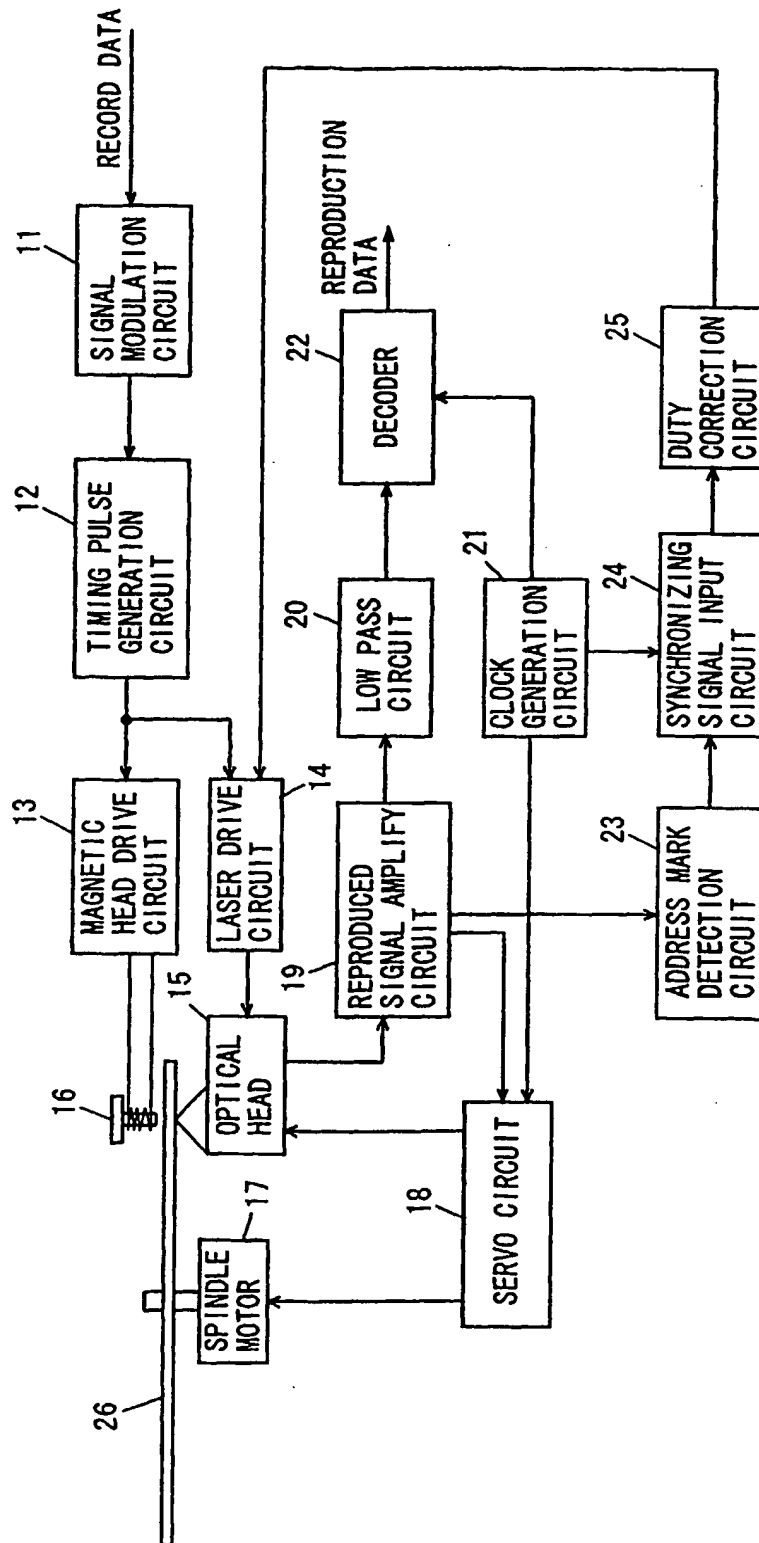
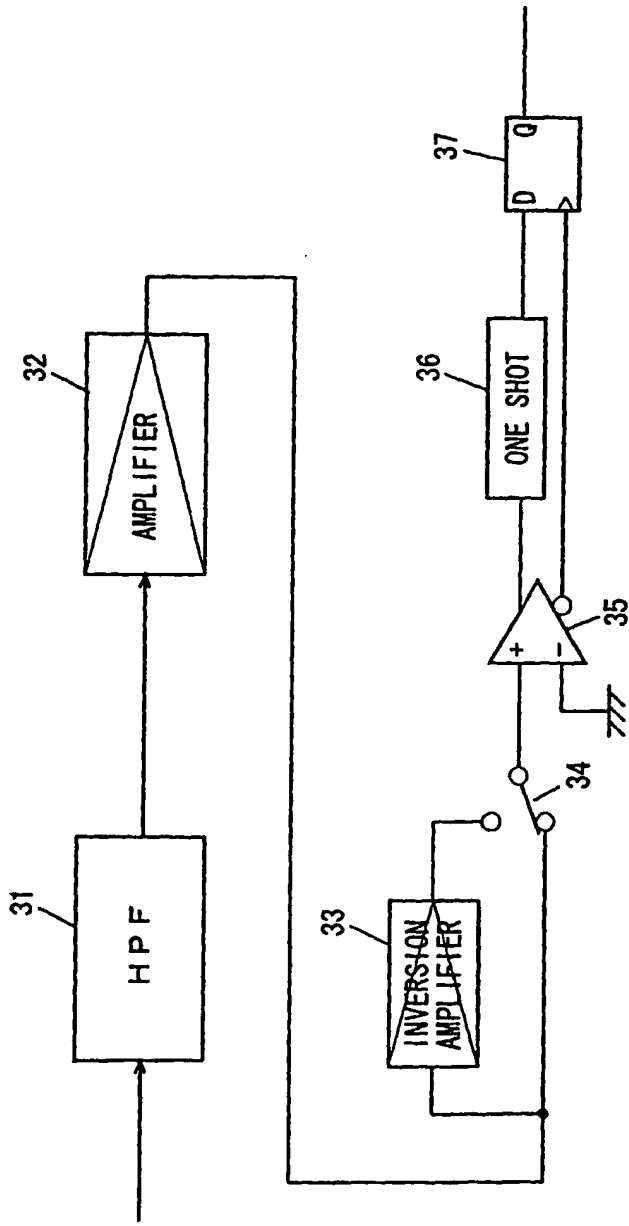


FIG. 10



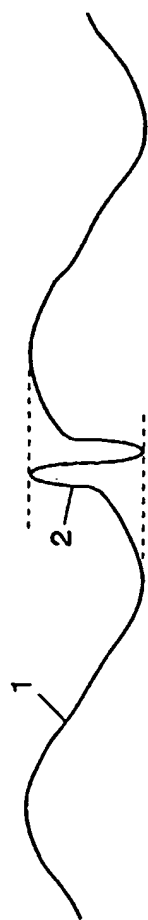


FIG. 11A

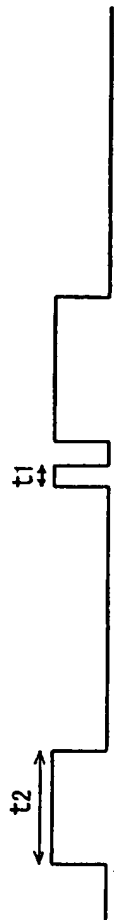


FIG. 11B

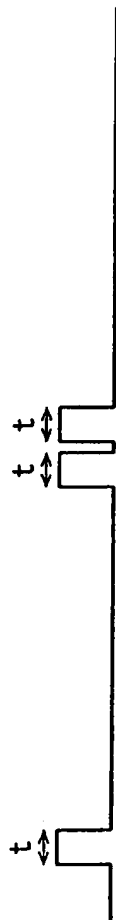


FIG. 11C



FIG. 11D



FIG. 11E

FIG. 12

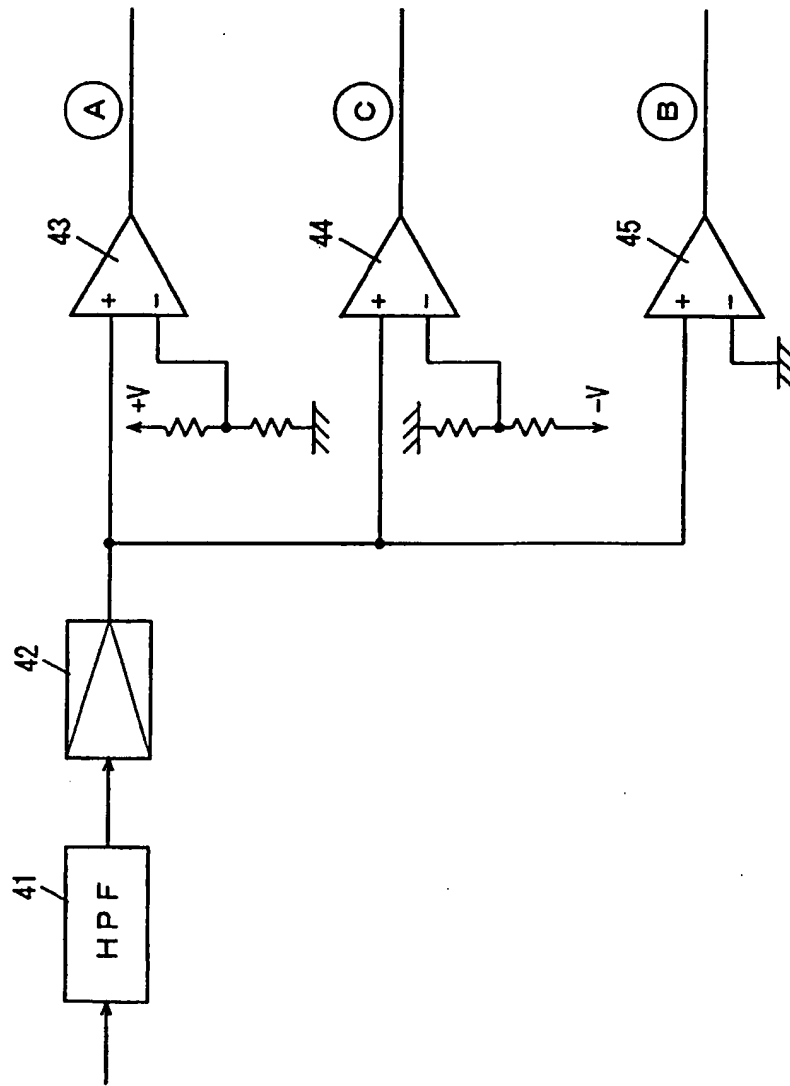
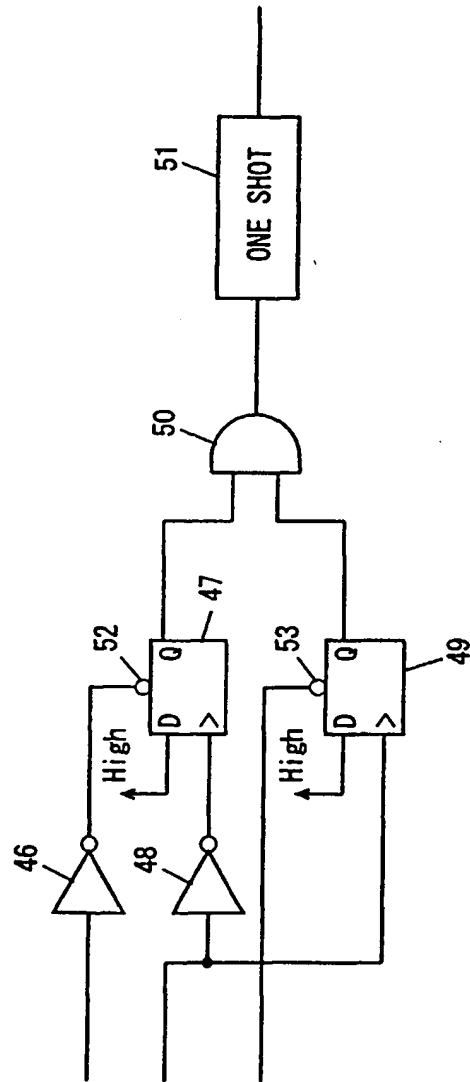
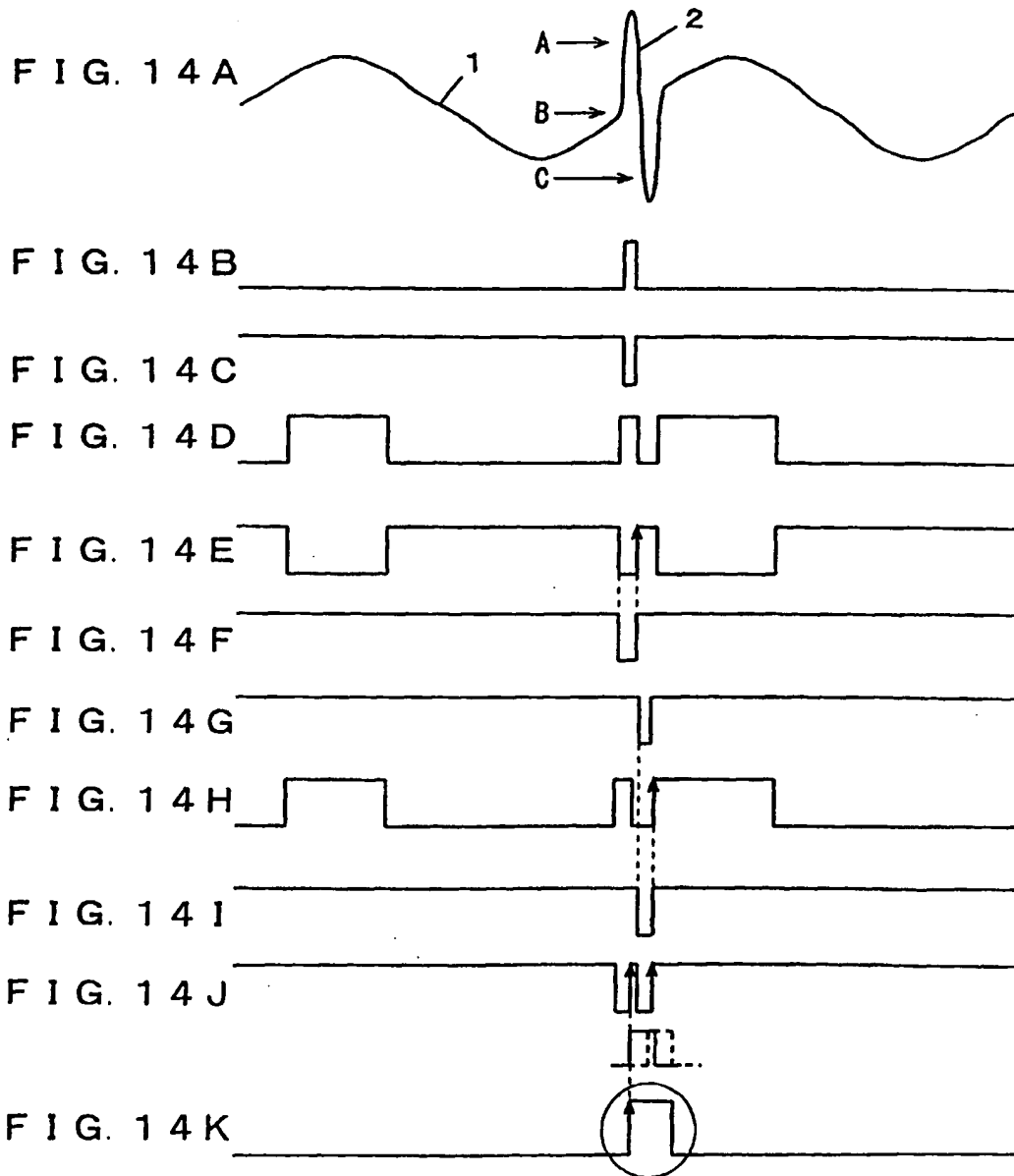


FIG. 13





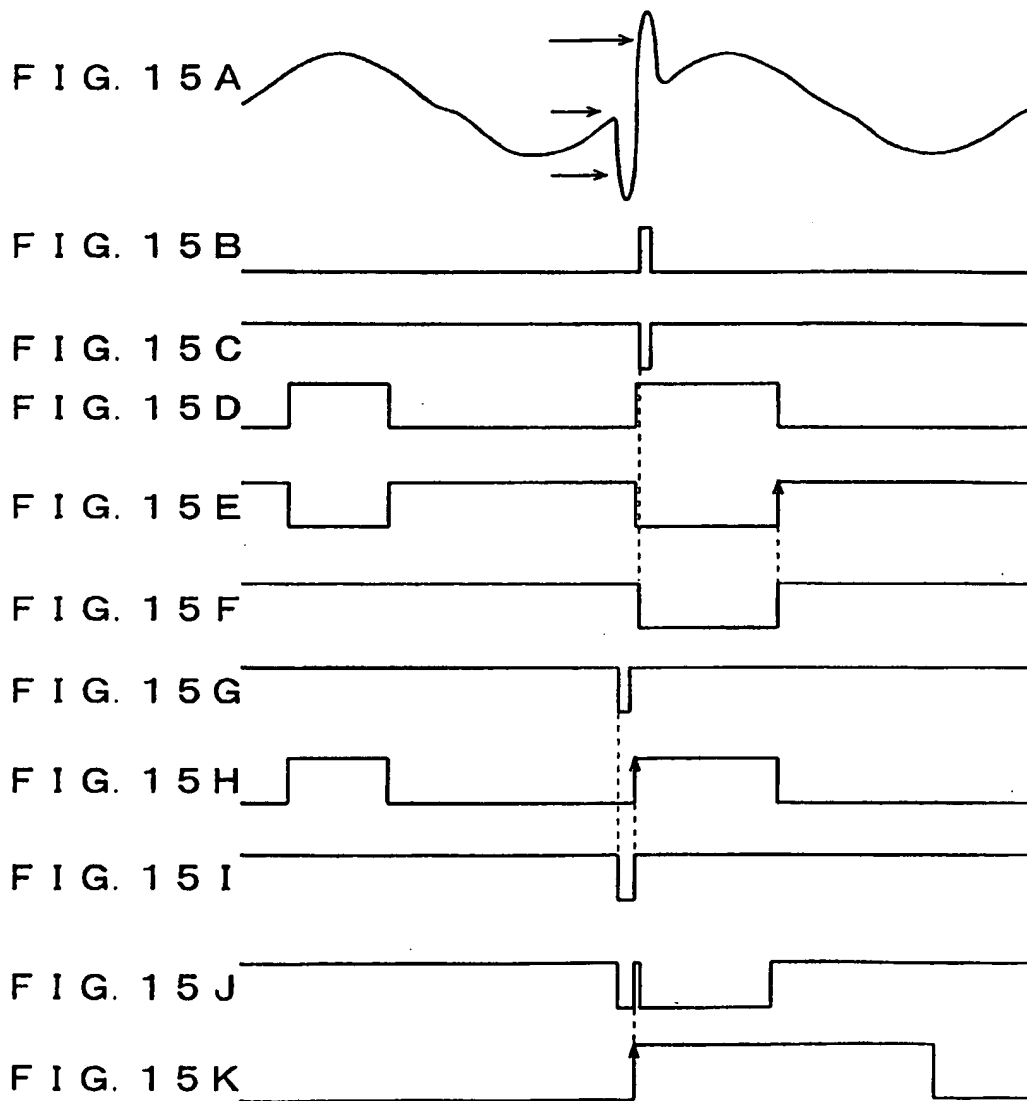


FIG. 16

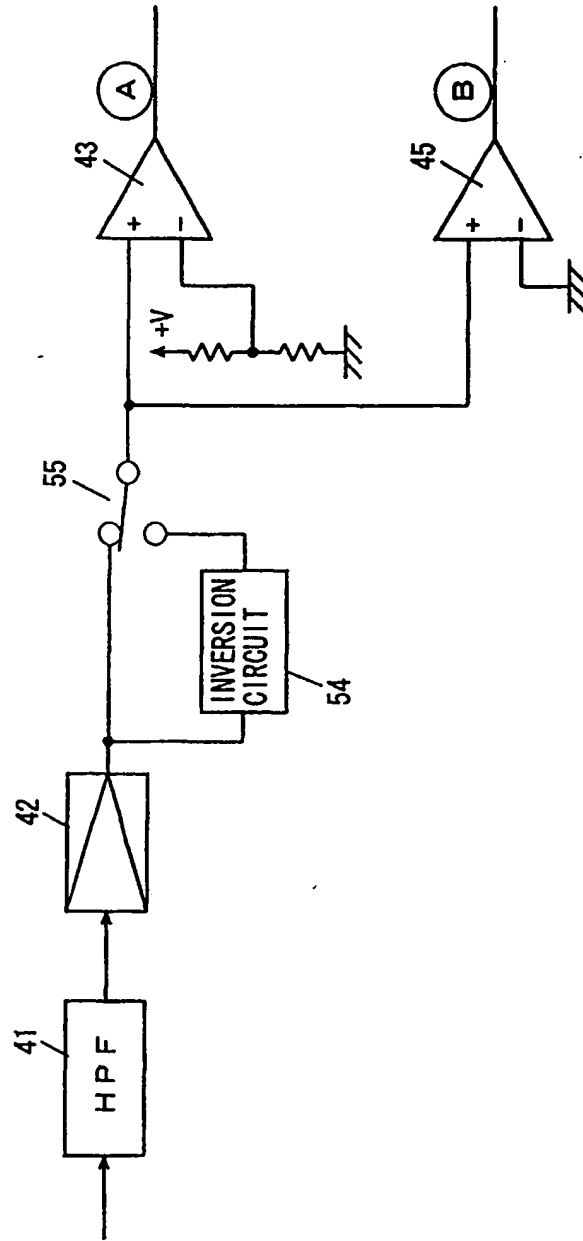
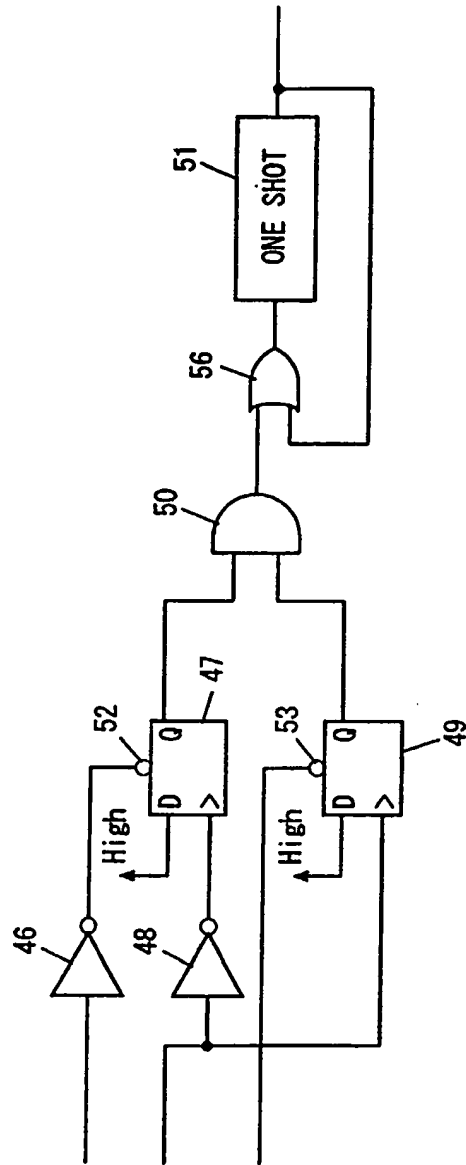


FIG. 17



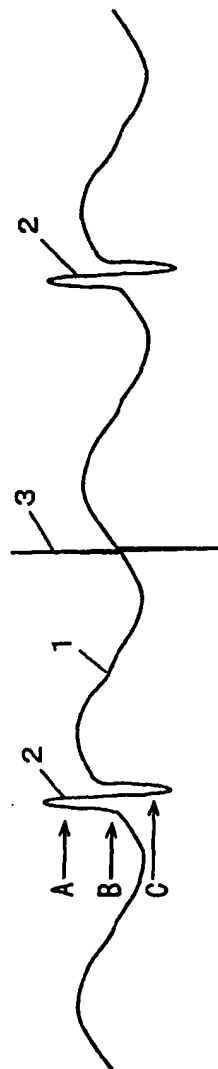


FIG. 18A

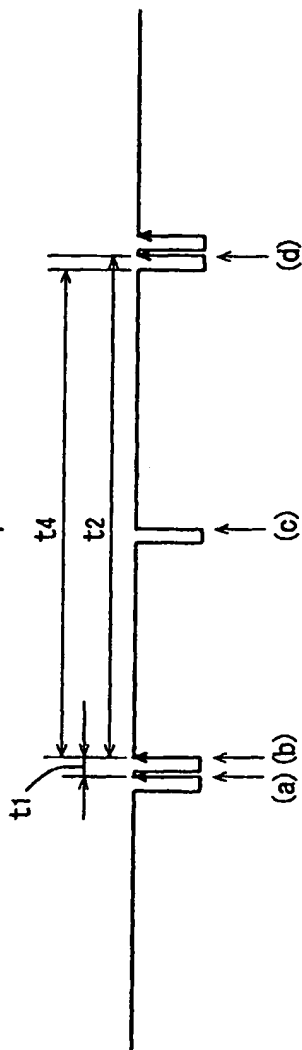


FIG. 18B



FIG. 18C



FIG. 18D

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP97/04743

A. CLASSIFICATION OF SUBJECT MATTER Int. Cl ⁶ G11B7/00, G11B11/10, G11B20/14 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) Int. Cl ⁶ G11B7/00, G11B11/10, G11B20/14 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Koho 1955 - 1998 Kokai Jitsuyo Shinan Koho 1971 - 1998 Toroku Jitsuyo Shinan Koho 1994 - 1998 Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, 1-223637, A (Mitsubishi Electric Corp.), September 6, 1989 (06. 09. 89) & US, 5070492, A	1, 2
X	JP, 64-1167, A (Hitachi, Ltd.), January 5, 1989 (05. 01. 89) (Family: none)	1, 2
A	JP, 8-339634, A (Sony Corp.), December 24, 1996 (24. 12. 96) (Family: none)	3 - 6
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search January 19, 1998 (19. 01. 98)		Date of mailing of the international search report January 27, 1998 (27. 01. 98)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.		Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)